FIG. 1 (Prior Art)

Translation of Macro Instructions into Native Instuctions

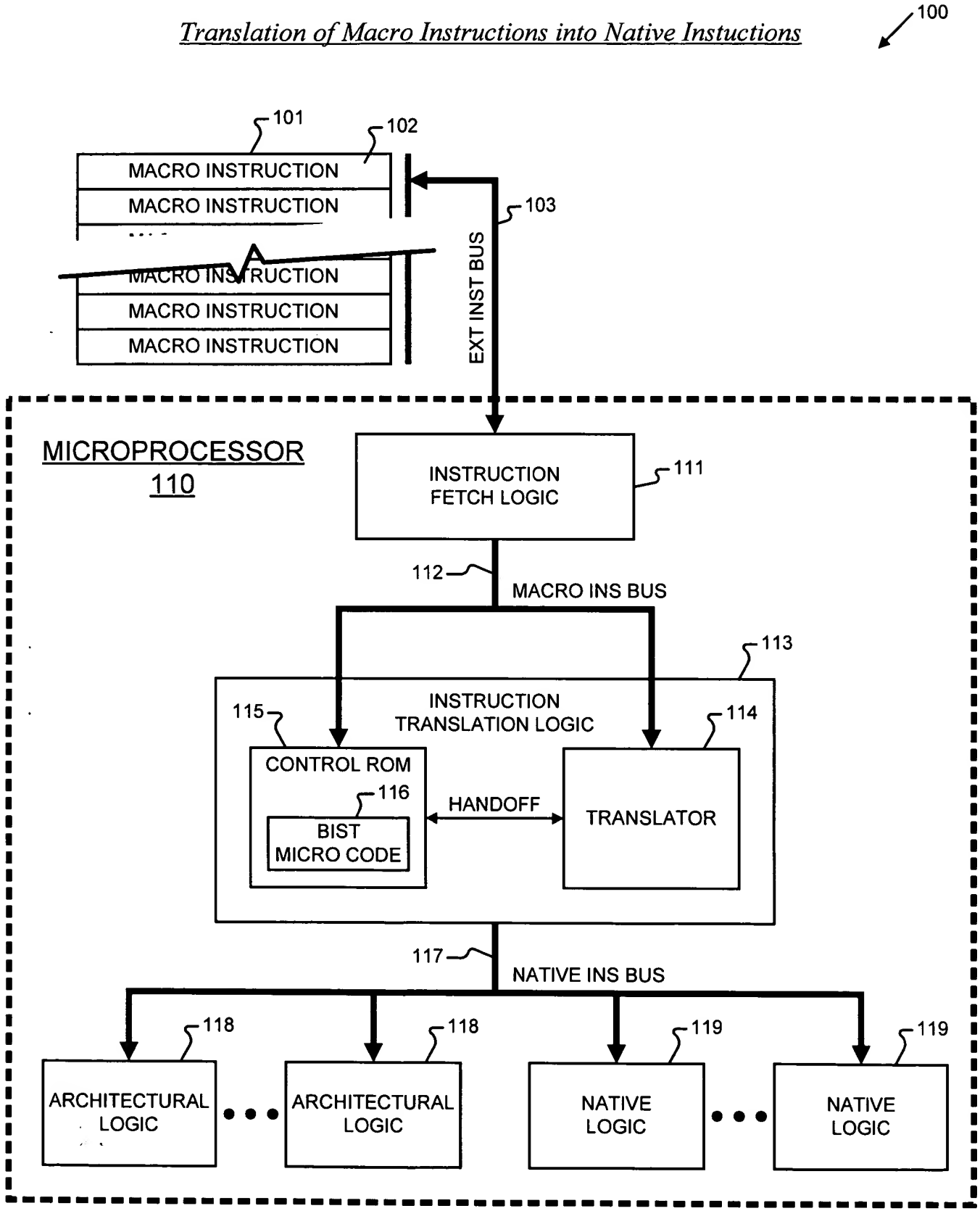

FIG. 2 (Prior Art)

Indirect Specification of Native Register via Macro Instruction

200

Cycle	Macro Ins Bus	Native Ins Bus
1	ADD [EAX],FFFFFFFFh	***
2	***	LD NR1,[EAX]
3	***	ADD NR1,NR1,FFFFFFFFh
4	***	ST [EAX],NR1

3 CYCLES

FIG. 3

Translator Bypass for Native Instructions

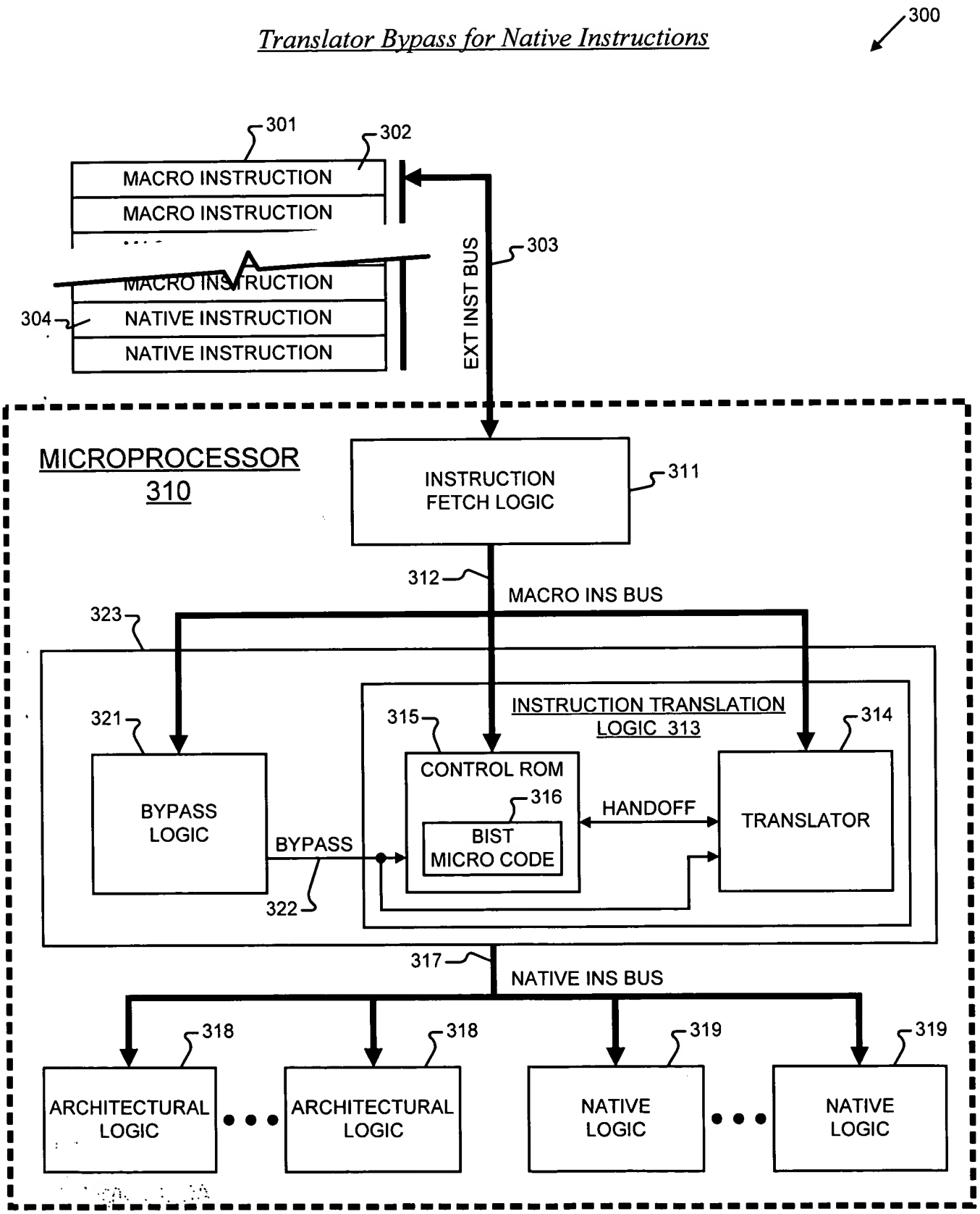

FIG. 4